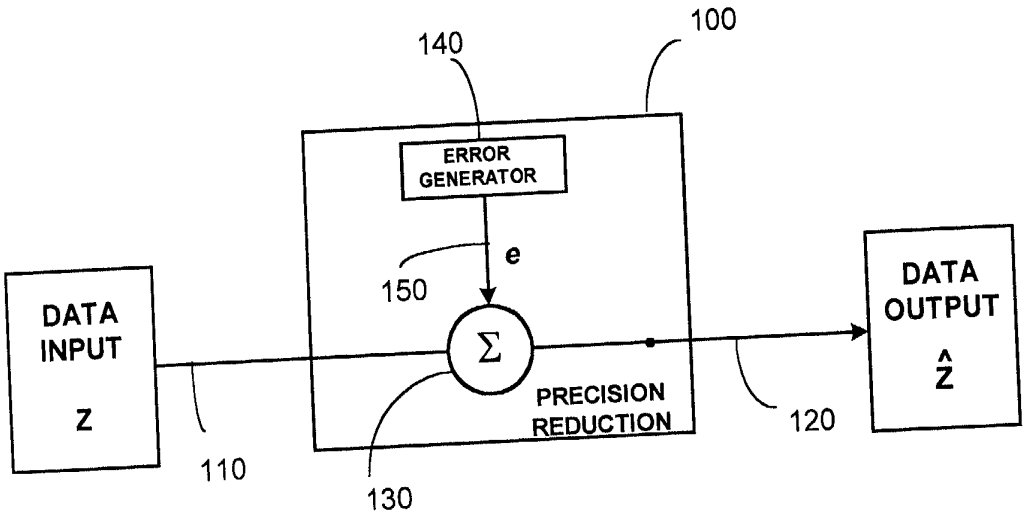

FIG. 1

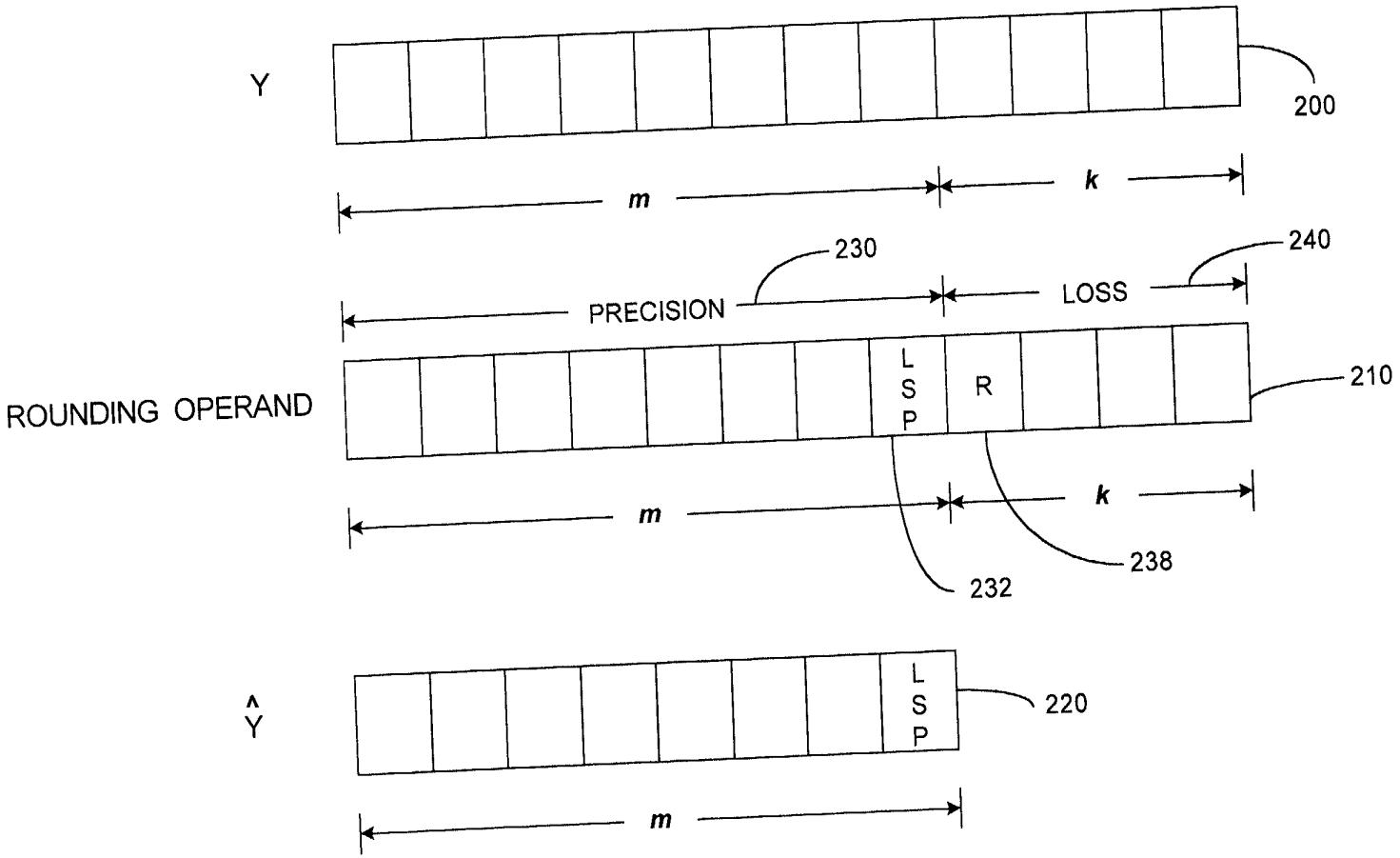
Y
200
m
k
230
240
PRECISION
LOSS
ROUNDING OPERAND
L
S
P
R
210
m
k
238
232
^
Y
L
S
P
220
m

FIG. 2A

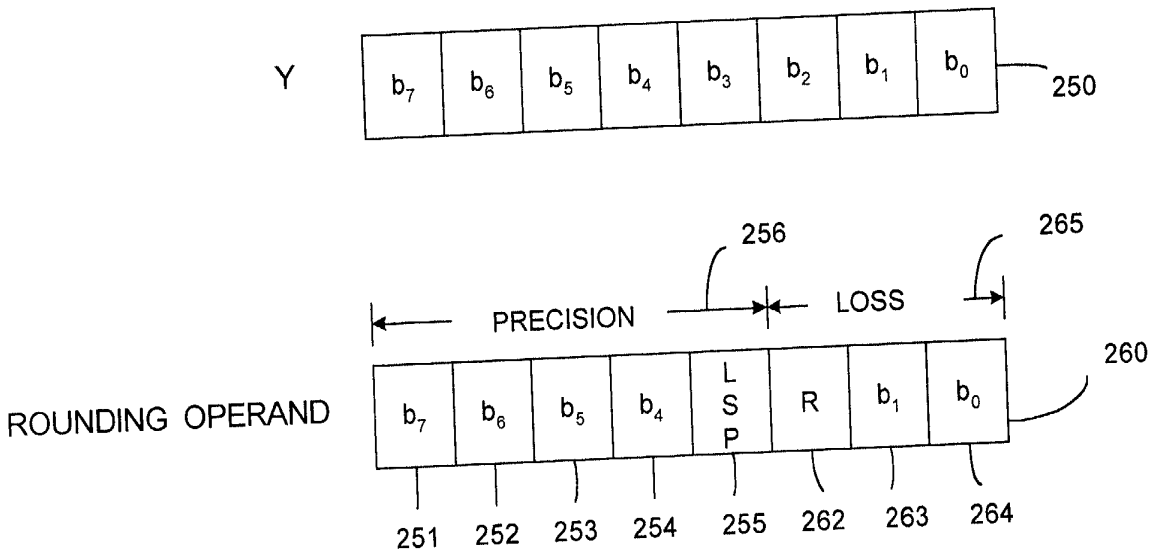
Y
b7 b6 b5 b4 b3 b2 b1 b0
250
256
265
PRECISION
LOSS
ROUNDING OPERAND
b7 b6 b5 b4 LSP R b1 b0
260
251 252 253 254 255 262 263 264
b7 b6 b5 b4
PRECISION
LSP
270
Ŷ

FIG. 2B

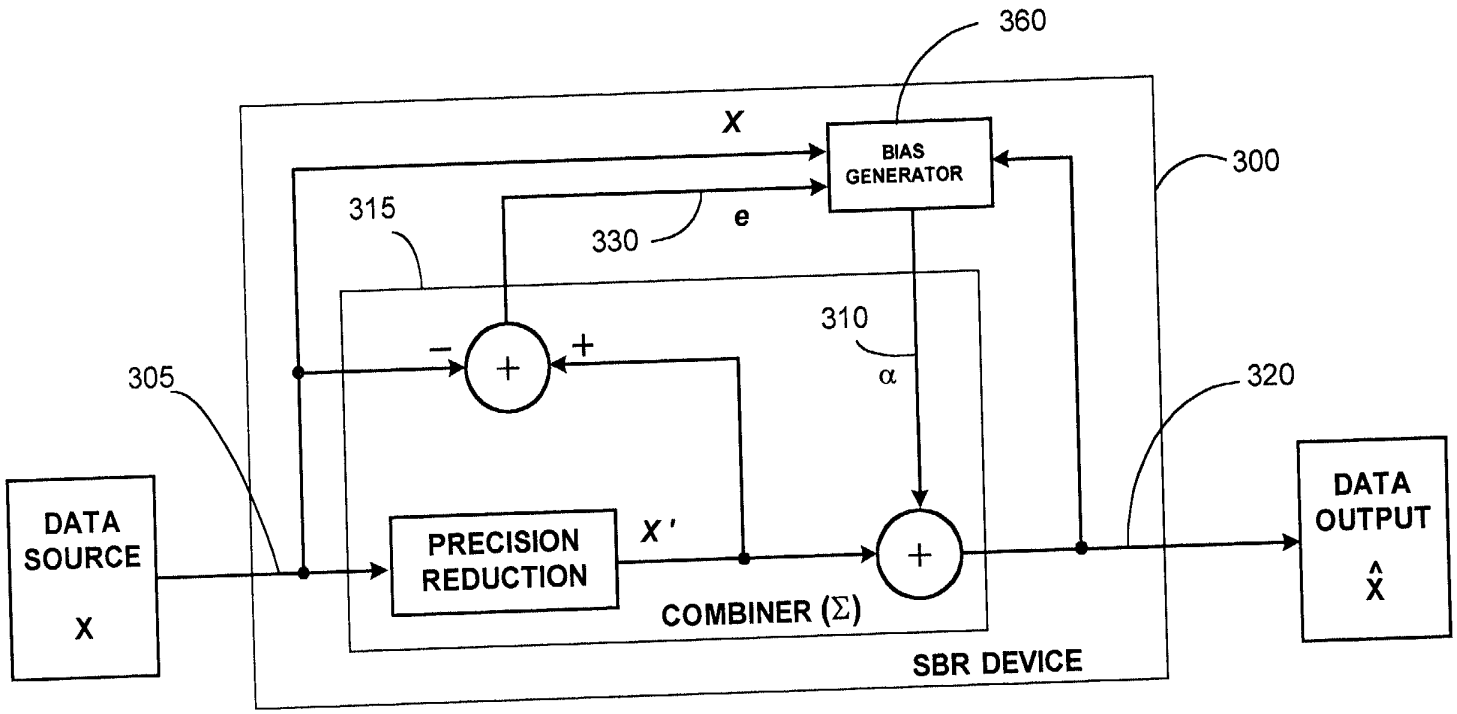

FIG. 3

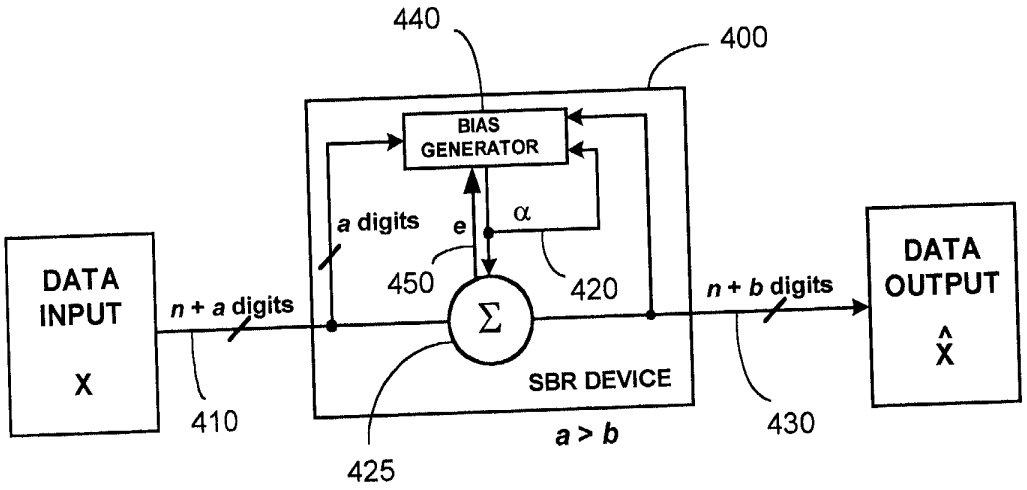

FIG. 4

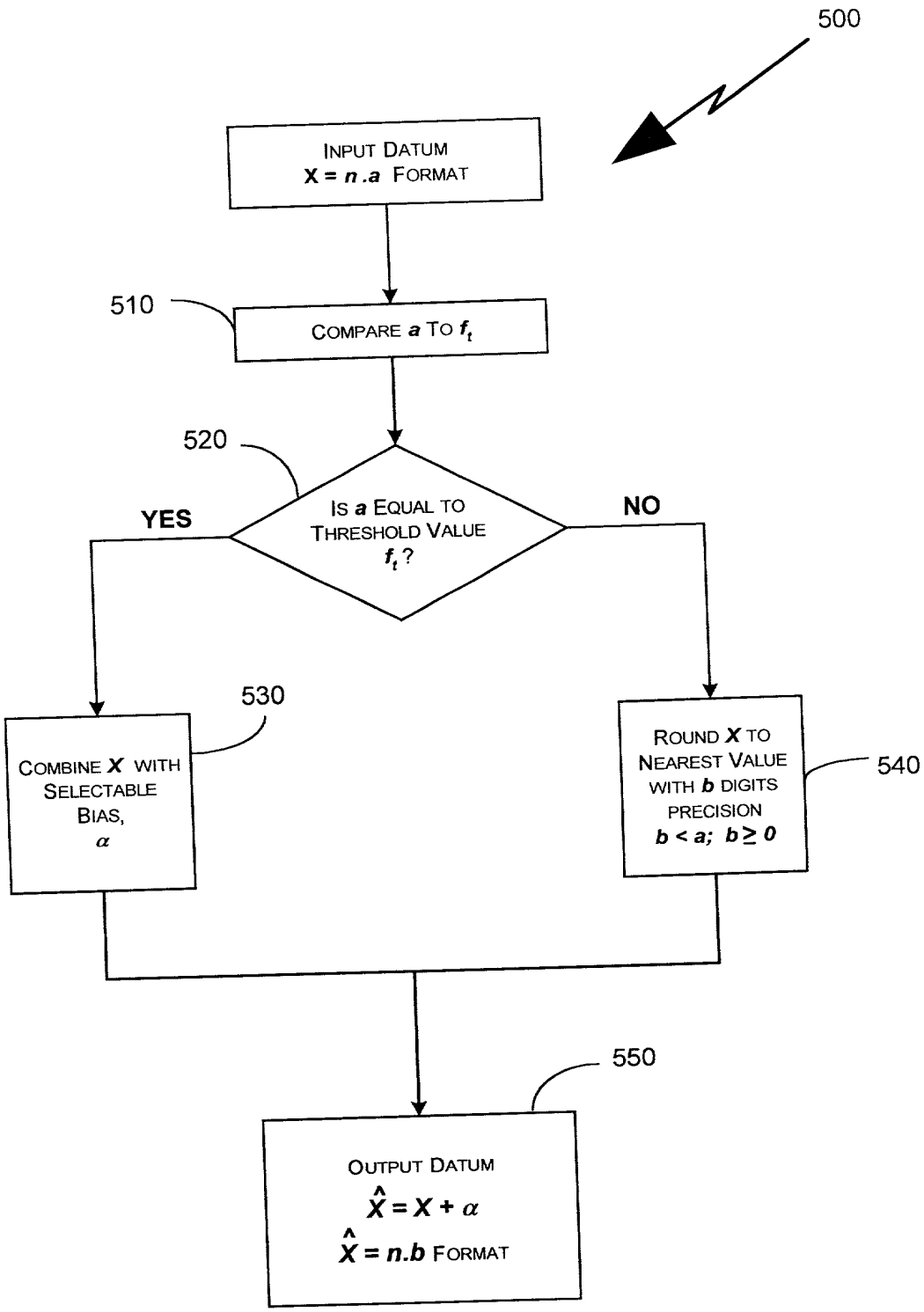
500
INPUT DATUM
X = n.a FORMAT
510
COMPARE a TO f_t
520
IS a EQUAL TO THRESHOLD VALUE f_t?
YES
NO
530
COMBINE X WITH SELECTABLE BIAS, α
ROUND X TO NEAREST VALUE WITH b DIGITS PRECISION
b < a; b ≥ 0
540
550
OUTPUT DATUM
$\hat{X} = X + \alpha$
$\hat{X}$ = n.b FORMAT

FIG. 5

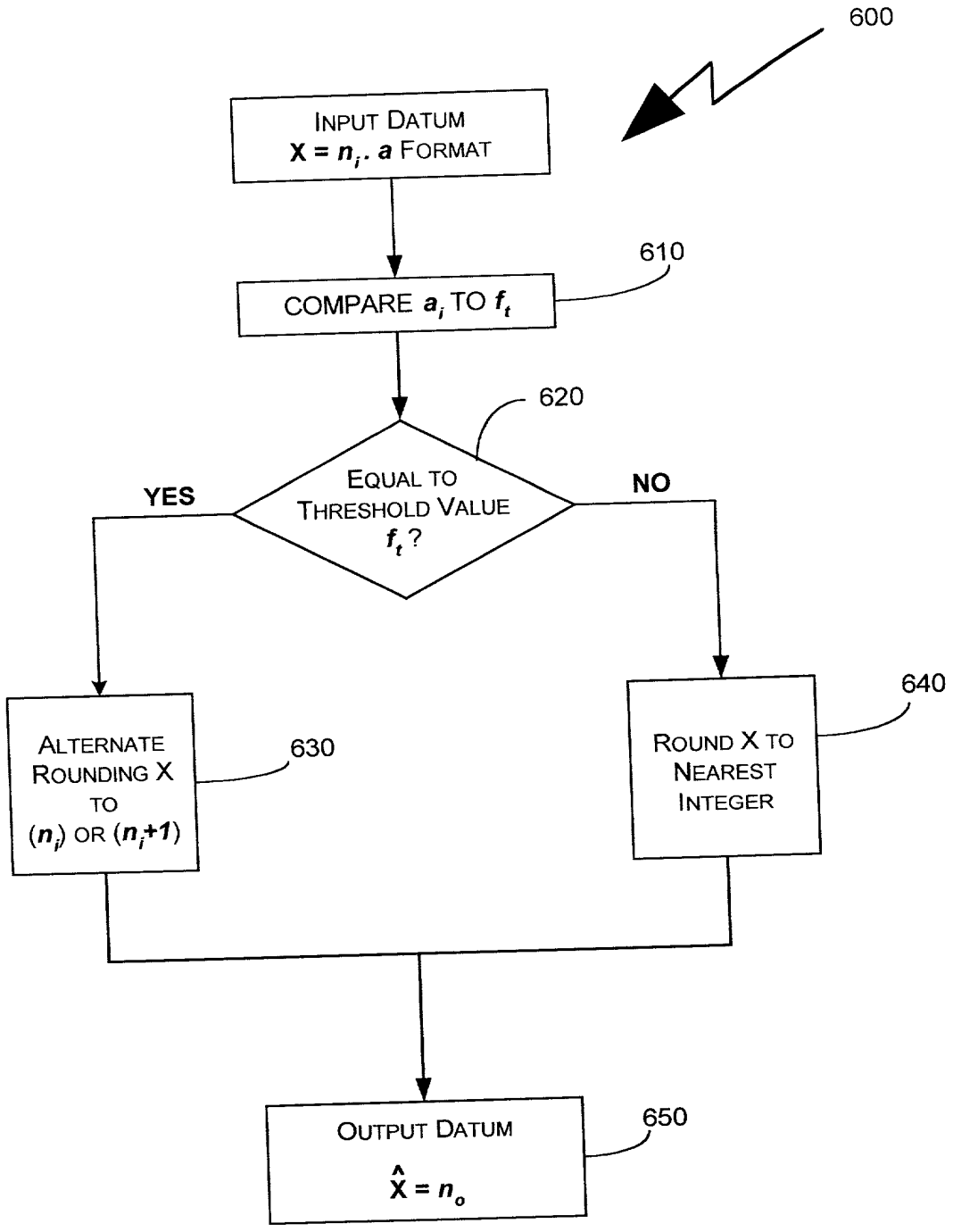
600
INPUT DATUM
X = n_i. a FORMAT
610
COMPARE a_i TO f_t
620
EQUAL TO THRESHOLD VALUE f_t?
YES
NO
ALTERNATE ROUNDING X TO (n_i) OR (n_i+1)
630
ROUND X TO NEAREST INTEGER
640
OUTPUT DATUM
$\hat{X} = n_o$
650

FIG. 6

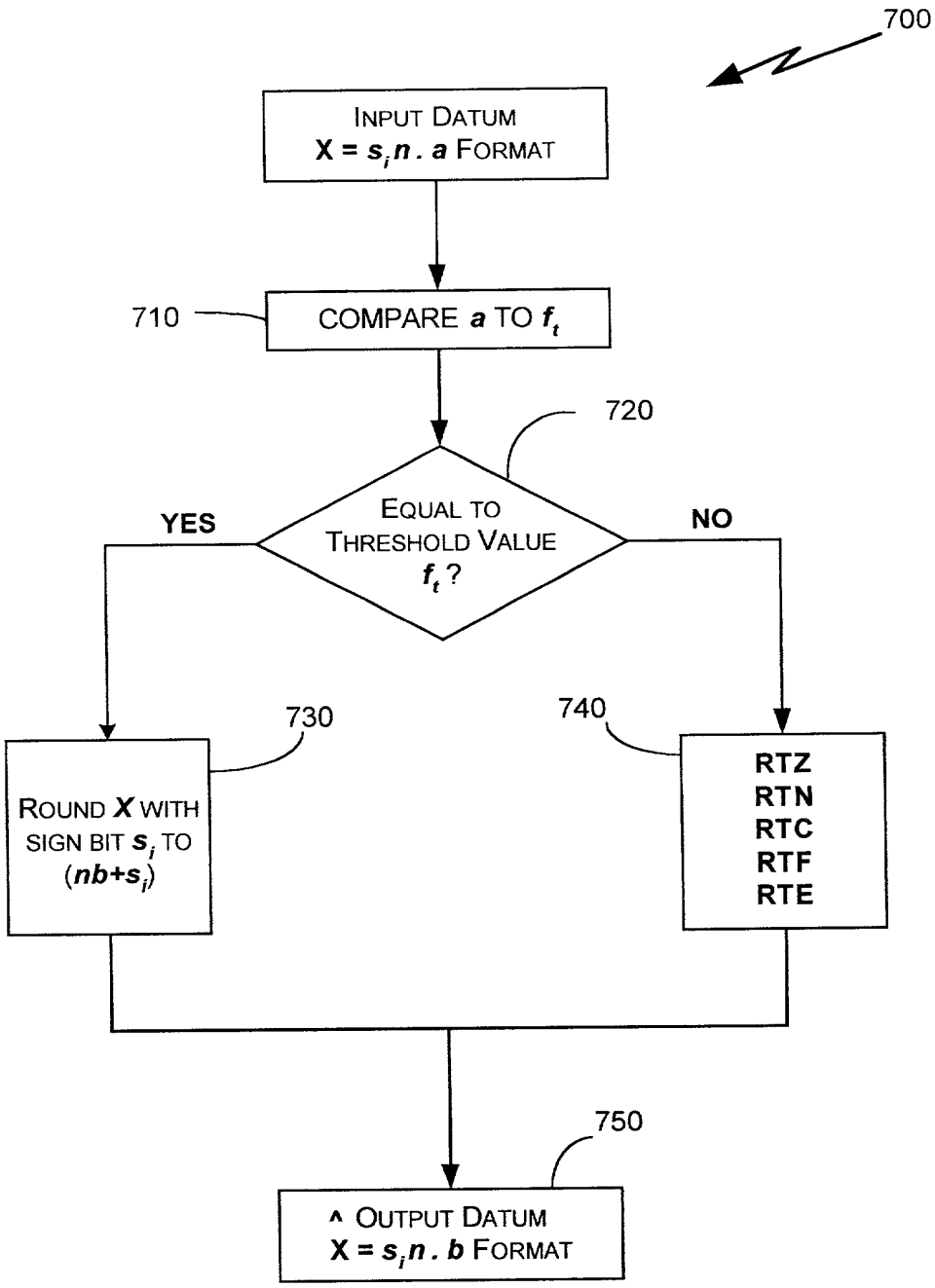
700
INPUT DATUM
X = s_i n . a FORMAT
710
COMPARE a TO f_t
720
EQUAL TO THRESHOLD VALUE f_t ?
YES
NO
730
ROUND X WITH SIGN BIT s_i TO (nb+s_i)
740
RTZ
RTN
RTC
RTF
RTE
750
^ OUTPUT DATUM
X = s_i n . b FORMAT

FIG. 7

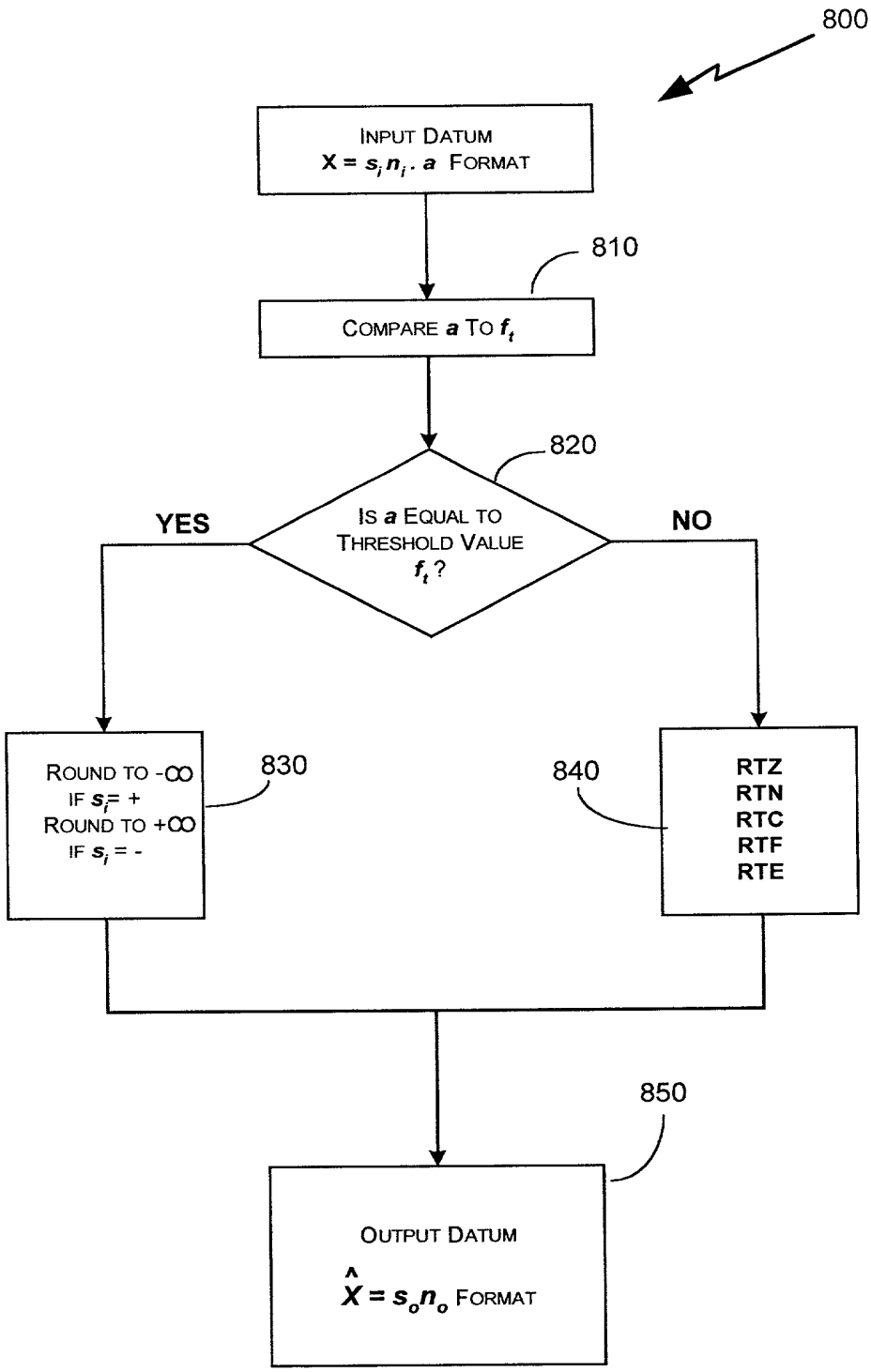
800
INPUT DATUM
X = $s_i n_i . a$ FORMAT
810
COMPARE a TO f_t
820
IS a EQUAL TO THRESHOLD VALUE f_t?
YES
NO
ROUND TO -∞ IF s_i = +
ROUND TO +∞ IF s_i = -
830
840
RTZ
RTN
RTC
RTF
RTE
850
OUTPUT DATUM
$\hat{X} = s_o n_o$ FORMAT

FIG. 8

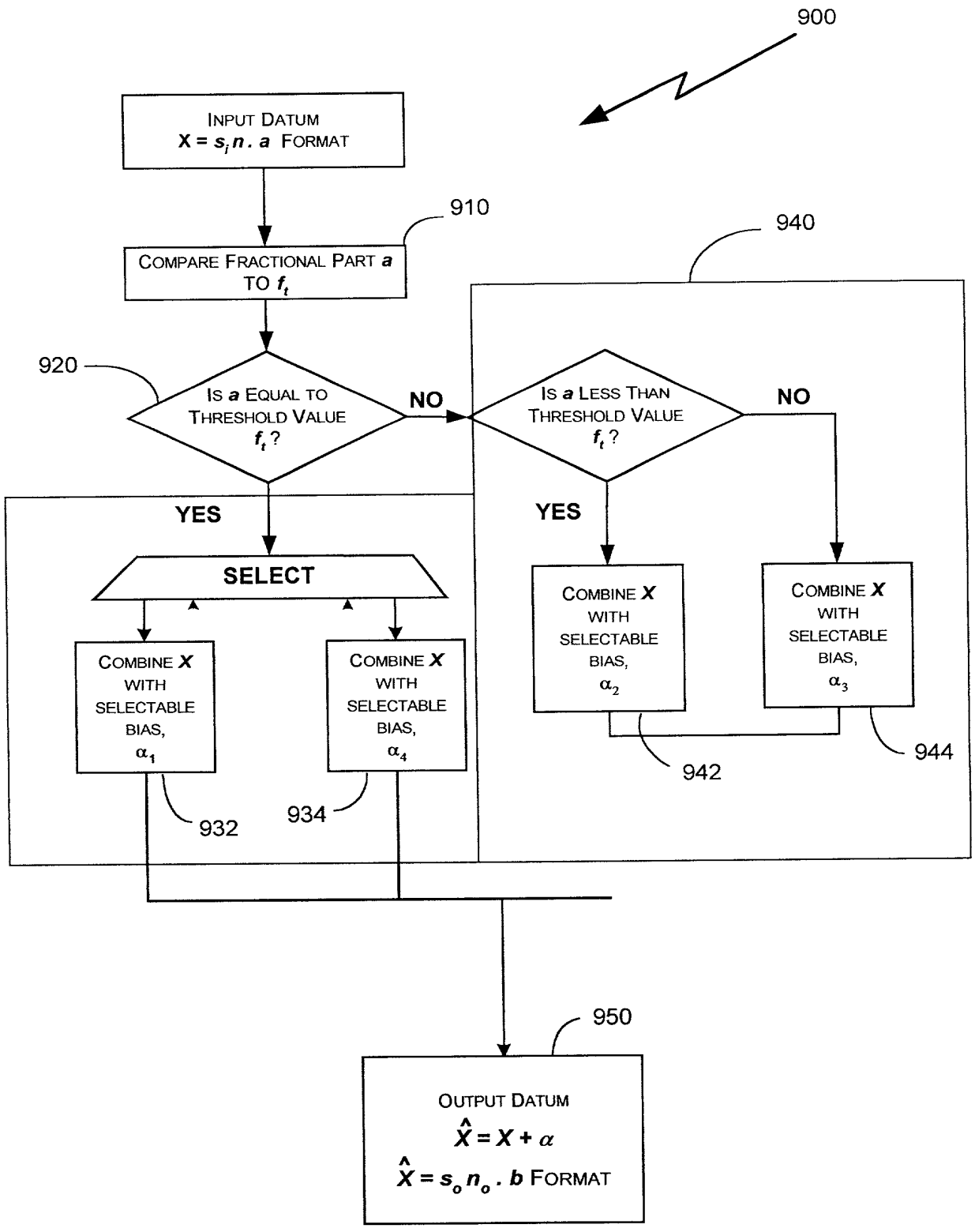
900
INPUT DATUM
X = s_i n . a FORMAT
910
COMPARE FRACTIONAL PART a TO f_t
940
920
IS a EQUAL TO THRESHOLD VALUE f_t ?
NO
IS a LESS THAN THRESHOLD VALUE f_t ?
NO
YES
YES
SELECT
COMBINE X WITH SELECTABLE BIAS, α_1
COMBINE X WITH SELECTABLE BIAS, α_4
COMBINE X WITH SELECTABLE BIAS, α_2
COMBINE X WITH SELECTABLE BIAS, α_3
932
934
942
944
950
OUTPUT DATUM
X̂ = X + α
X̂ = s_o n_o . b FORMAT

FIG. 9

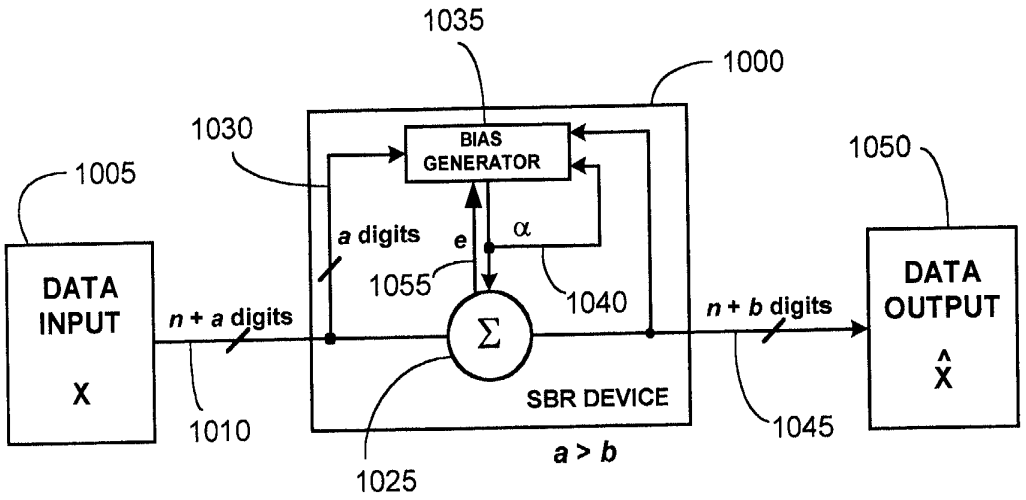
1035
1000
1030
BIAS GENERATOR
1050
1005
a digits
e
α
DATA INPUT
X
1055
1040
n + a digits
Σ
n + b digits
DATA OUTPUT
X̂
SBR DEVICE
1010
1045
a > b
1025

FIG. 10

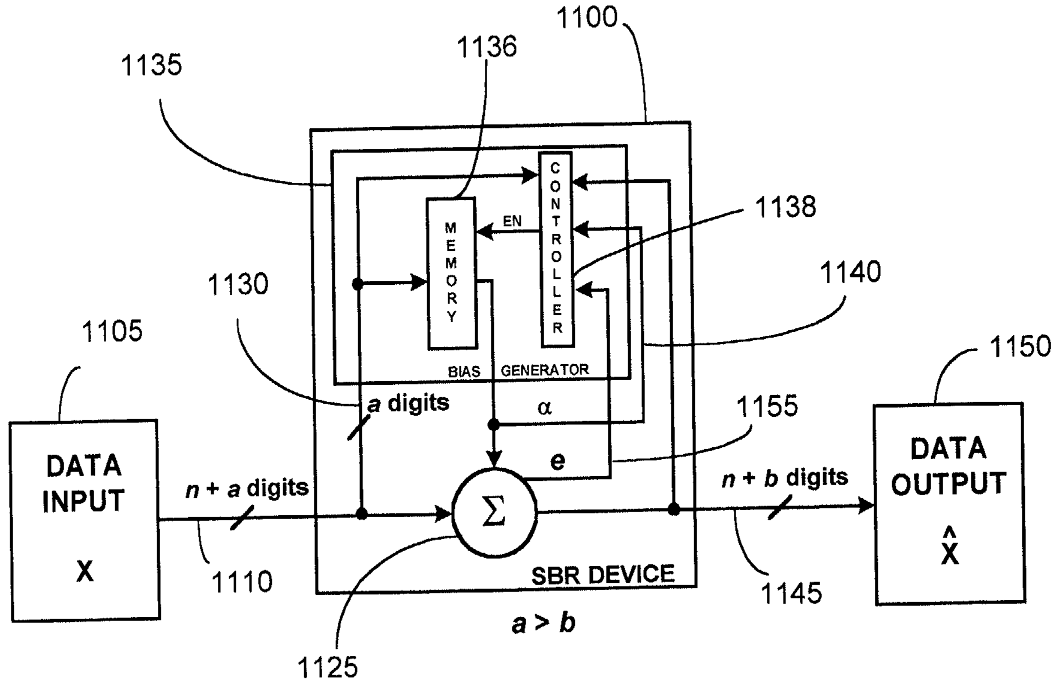
1100
1135
1136
1138
1140
1130
1105
1150
1155
1110
1145
1125
DATA INPUT
X
n + a digits
a digits
MEMORY
CONTROLLER
EN
BIAS GENERATOR
α
e
Σ
SBR DEVICE
a > b
n + b digits
DATA OUTPUT
X̂

FIG. 11

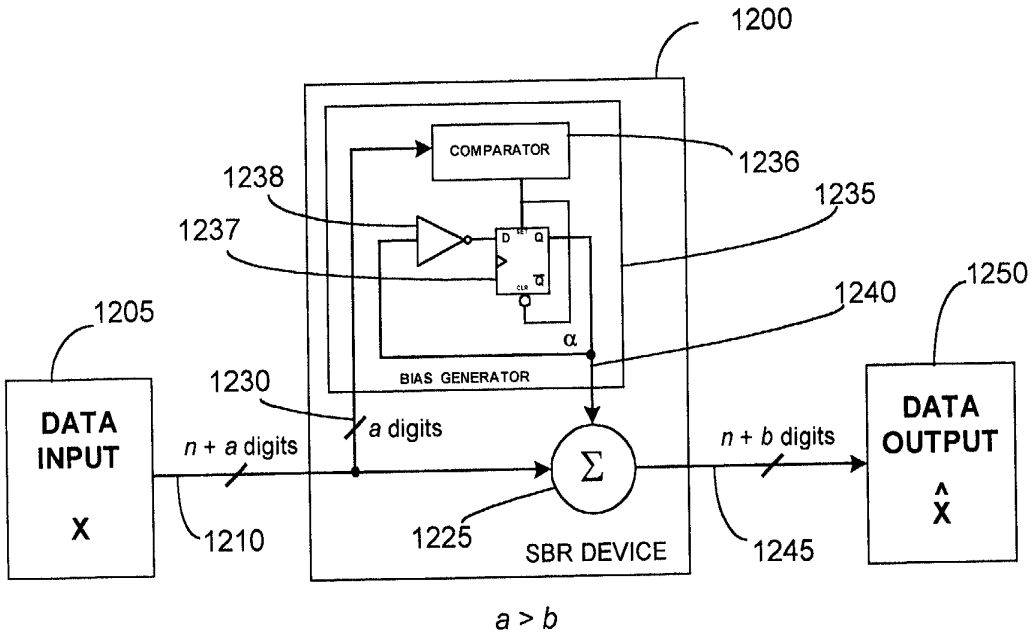
1200
COMPARATOR
1236
1238
1235
1237
1240
1250
1205
α
BIAS GENERATOR
1230
DATA
INPUT
X
a digits
n + a digits
n + b digits
DATA
OUTPUT
X̂
Σ
1210
1225
SBR DEVICE
1245
a > b

FIG. 12

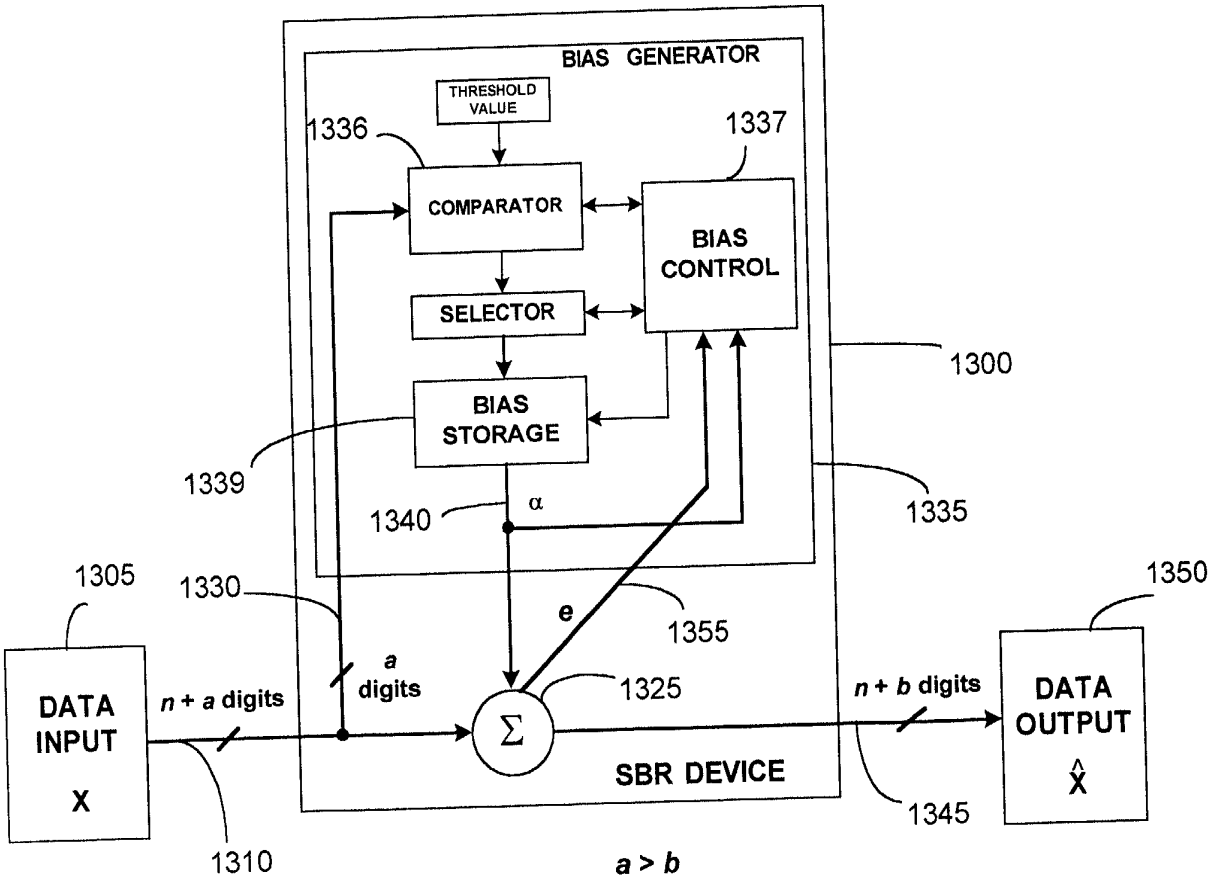

FIG. 13

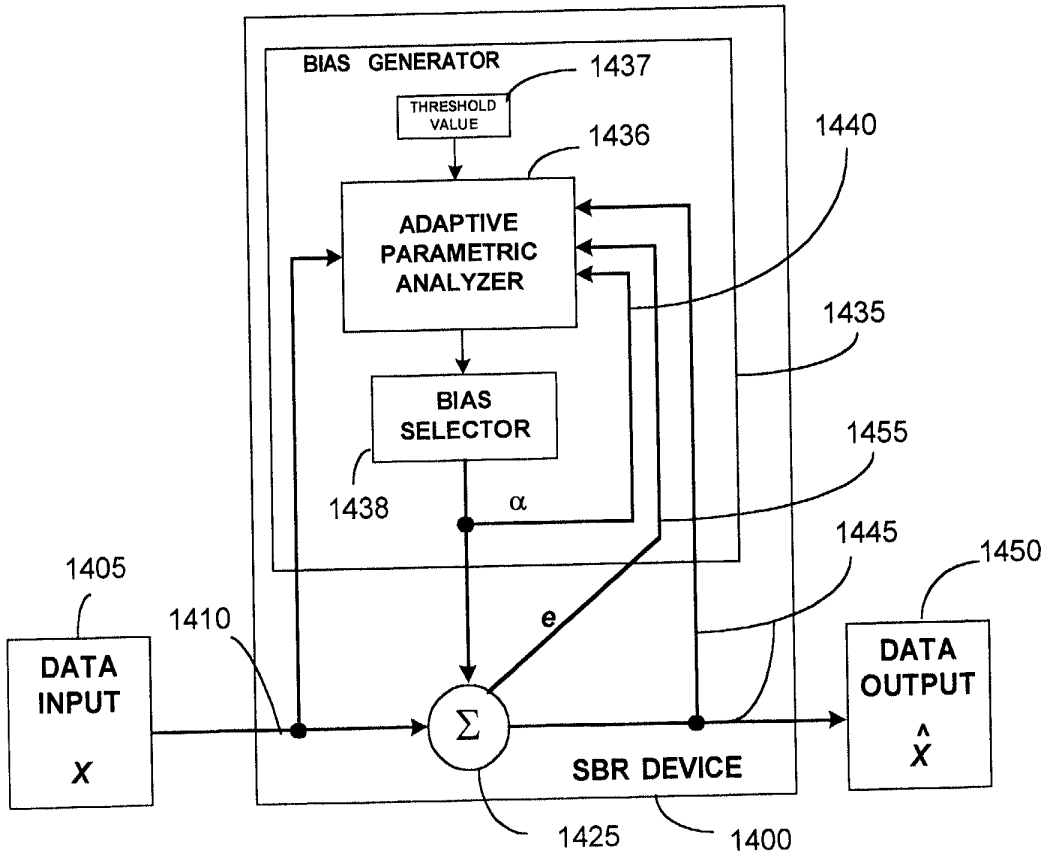

FIG. 14

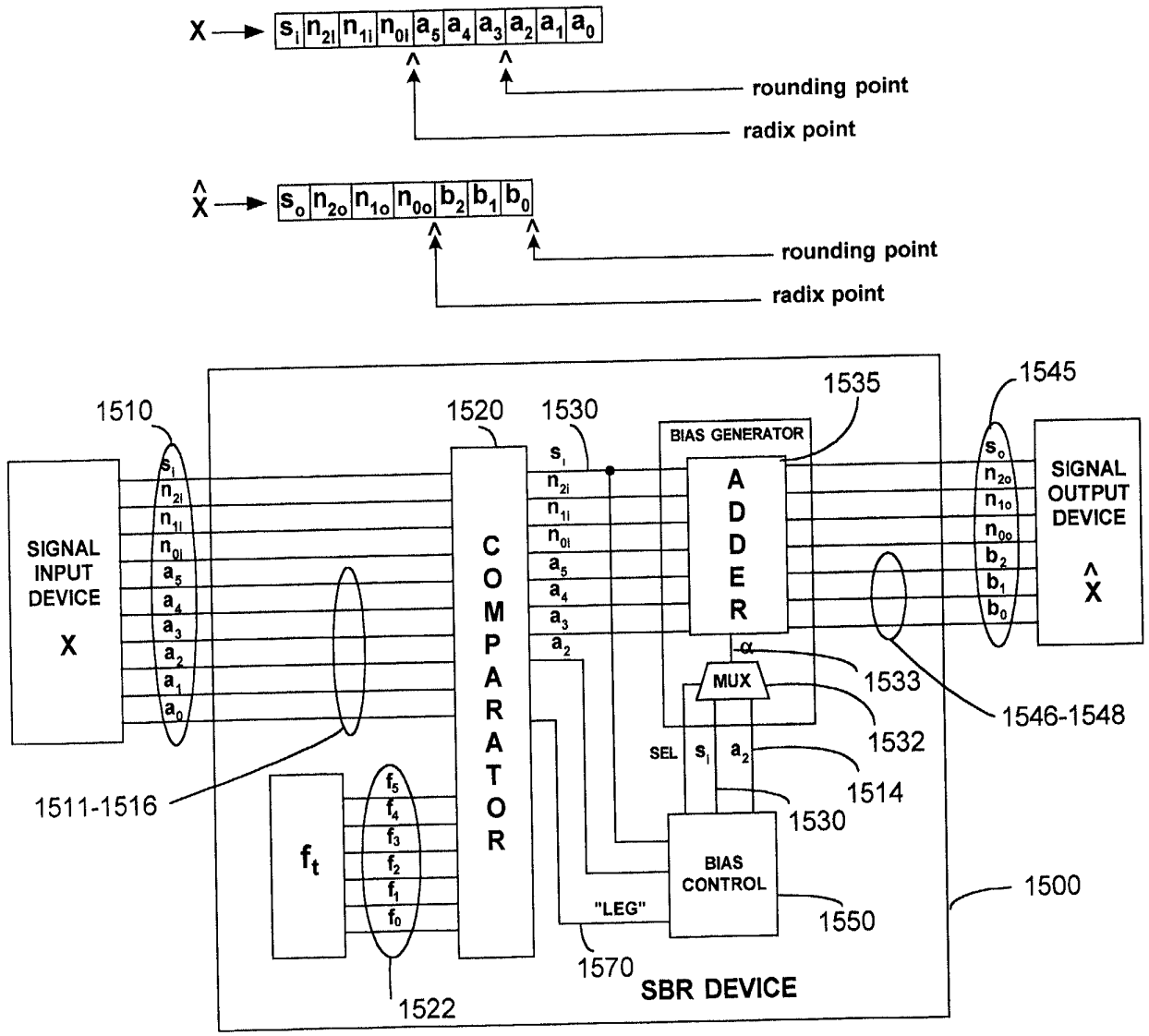
X
s_i n_{2i} n_{1i} n_{0i} a_5 a_4 a_3 a_2 a_1 a_0
rounding point
radix point
$\hat{X}$
s_o n_{2o} n_{1o} n_{0o} b_2 b_1 b_0
rounding point
radix point
1510
1520
1530
1535
1545
SIGNAL INPUT DEVICE
X
COMPARATOR
BIAS GENERATOR
ADDER
MUX
SEL
BIAS CONTROL
"LEG"
SIGNAL OUTPUT DEVICE
$\hat{X}$
f_t
1511-1516
1522
1533
1532
1514
1530
1546-1548
1550
1570
1500
SBR DEVICE

FIG. 15

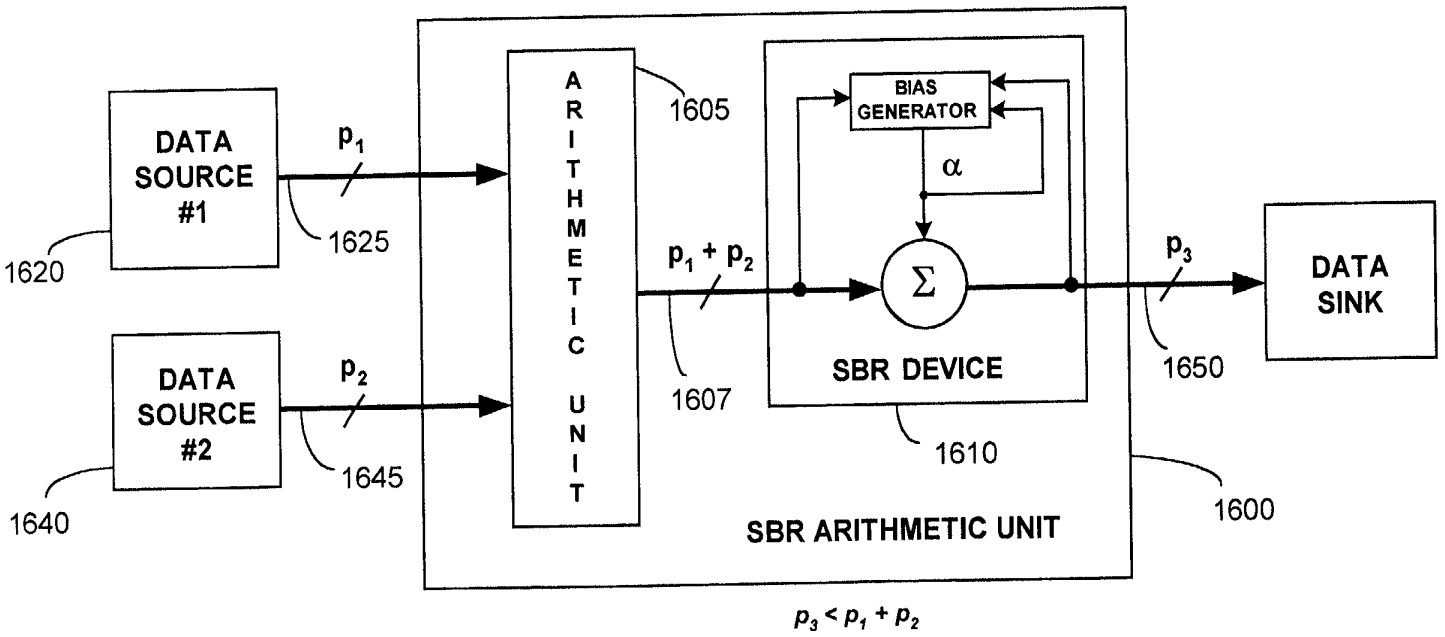
DATA SOURCE #1
1620
p_1
1625
DATA SOURCE #2
1640
p_2
1645
ARITHMETIC UNIT
1605
$p_1 + p_2$
1607
BIAS GENERATOR
α
Σ
SBR DEVICE
1610
p_3
1650
DATA SINK
SBR ARITHMETIC UNIT
1600
$p_3 < p_1 + p_2$

FIG. 16

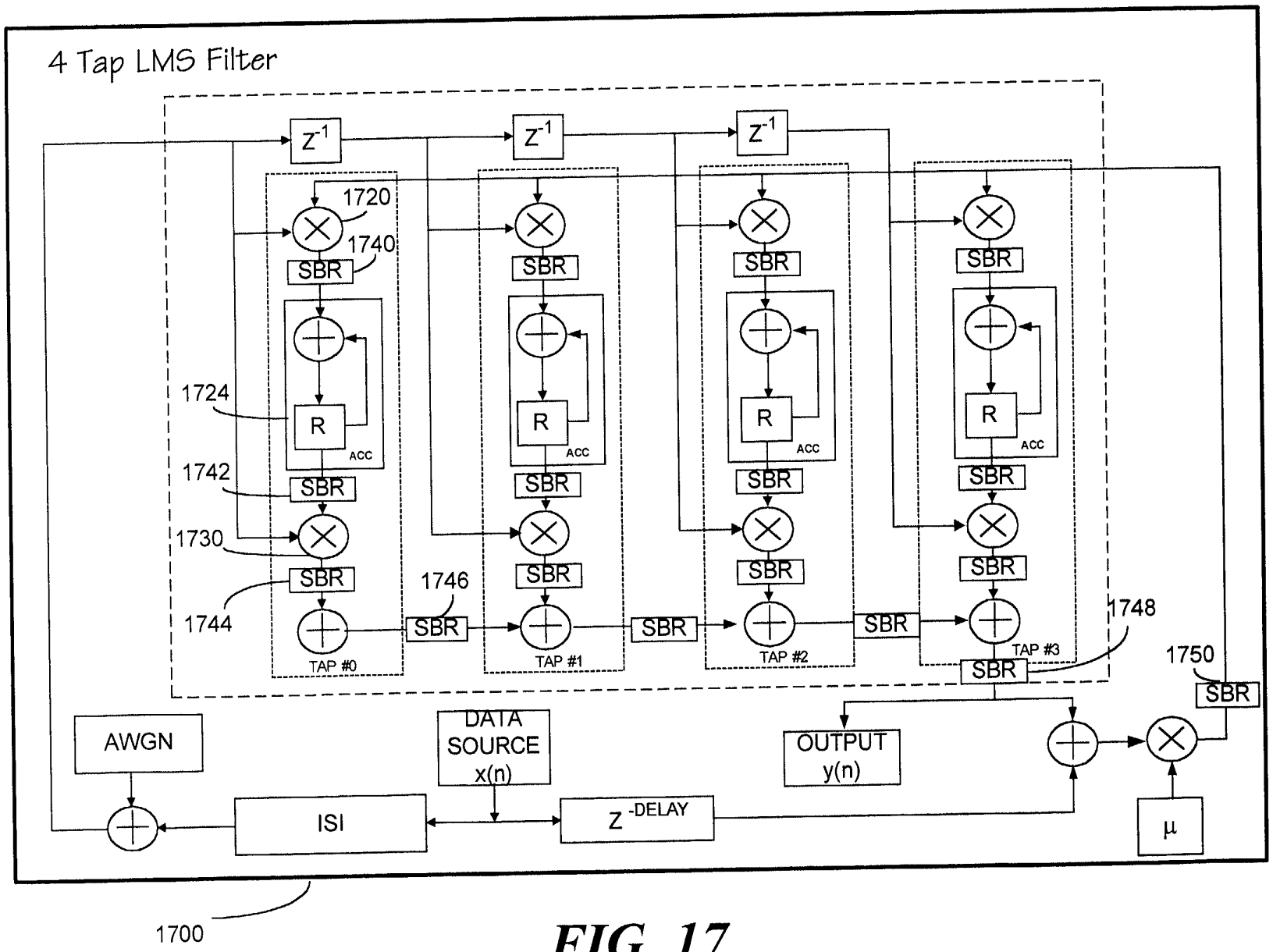
4 Tap LMS Filter
Z-1
Z-1
Z-1
1720
1740
SBR
1724
R
ACC
1742
1730
1744
1746
1748
1750
TAP #0
TAP #1
TAP #2
TAP #3
AWGN
DATA SOURCE x(n)
OUTPUT y(n)
ISI
Z -DELAY
μ
1700

FIG. 17